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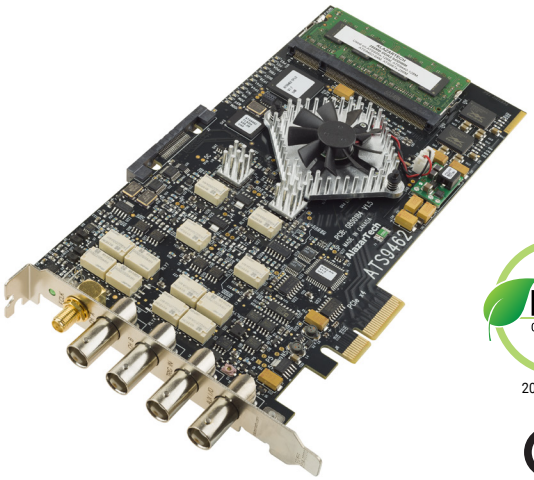
AlazarTech

ATS9462

180 MS/s 16-Bit PCI Express Digitizer

- 720 MB/s PCI Express (4-lane) interface
- 2 channels sampled at 16-bit resolution
- 180 MS/s simultaneous real-time sampling rate on each input
- ±200 mV to ±16 V input range
- On-board dual-port memory up to 512 Megasamples per channel
- FPGA-based input processing engine
- AlazarDSO® oscilloscope software
- Software Development Kit supports C/C++, C#, Python, MATLAB®, LabVIEW®
- Support for Windows® & Linux®



RoHS 3 COMPLIANT
2015/863/EU

CE

Product	Bus	Operating System	Channels	Max. Sample Rate	Bandwidth	Memory Per Channel	Resolution
ATS9462	PCIe x4	32-bit/64-bit Windows & 64-bit Linux	2	180 MS/s	65 MHz	64M, 512M	16 bits

Overview

AlazarTech ATS®9462 is a 4-lane PCI Express (PCIe x4), dual-channel, high-resolution, 16-bit, 180 MS/s waveform digitizer card capable of streaming acquired data to PC memory at rates up to 720 MB/s.

ATS9462 is available with up to 512 Megasamples of on-board, dual-port memory per channel. This memory can be used as a very deep FIFO to mitigate system latencies during sustained data transfer.

Users can capture data from one trigger or a burst of triggers. Users can also stream very large datasets continuously to PC memory or hard disk.

ATS9462 allows users to build real-time data acquisition systems even under the Windows or Linux operating systems, as users are allowed to read acquired data while the next acquisition is in progress.

ATS9462 PCI digitizers are an ideal solution for cost-sensitive OEM applications that require a digitizer to be embedded into the customer's equipment.

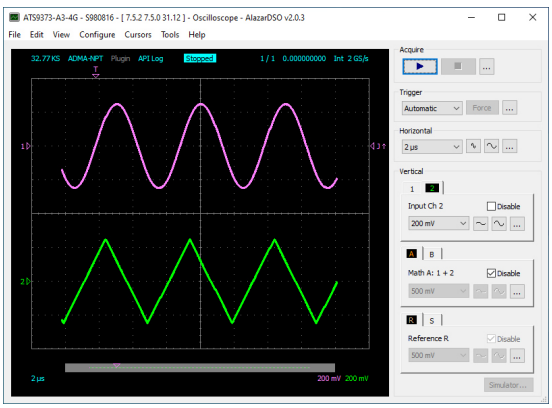
ATS9462 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who need to integrate the ATS9462 in their own program can purchase a software development kit, ATS-SDK, for C/C++, C#, Python, MATLAB, and LabVIEW for both Windows and Linux operating systems.

All of this advanced functionality is packaged in a low-power, half-length PCI Express card.

Applications

Optical Coherence Tomography (OCT)
Ultrasonic & Eddy Current NDT/NDE
Radar/RF Signal Recording
Terabyte Storage Oscilloscope
High-Resolution Oscilloscope
Spectroscopy
Multi-Channel Transient Recording



PCI Express Bus Interface

ATS9462 interfaces to the host computer using a 4-lane PCI Express bus. Each lane operates at 2.5 Gbps. PCIe bus specification v1.0a and v1.1 are supported.

According to PCIe specification, a 4-lane board can be plugged into any 4-lane, 8-lane or 16-lane slot, but not into a 1-lane slot. As such, ATS9462 requires at least one free 4-lane, 8-lane or 16-lane slot on the motherboard.

The physical and logical PCIe x4 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and acquisition datapath. This very high degree of integration allows for optimum product reliability.

The AlazarTech® 720 MB/s benchmarks were done using an ASUS® WS X299 SAGE motherboard.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. AlazarTech, on the other hand, specifies the benchmarked sustained throughput. To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed.

Analog Input

An ATS9462 features two analog input channels with extensive functionality. Each channel has 65 MHz of full power analog input bandwidth. With software-selectable attenuation, you can achieve an input voltage range of ±200 mV to ±16 V. Attenuating probes (not included) can extend the voltage range even higher.

Software-selectable AC or DC coupling further increases the signal measurement capability. Software-selectable 50 Ω input impedance makes it easy to interface to high-speed RF signals.

Amplifier Bypass Mode

To obtain optimum dynamic performance, choose the Amplifier Bypass Mode. This mode comes standard with the ATS9462. Each channel can be independently bypassed using on-board DIP-switches.

Once the amplifier has been bypassed, the input for that channel has 50 Ω impedance, DC coupling and a ±800 mV full scale input range. Diode protection is still included, but users should avoid saturation of the input beyond 120% of full scale.

Wideband Input Upgrade

Some applications, such as Digital Video Broadcast (DVB), require analog input bandwidth to be higher than the standard bandwidth of ATS9462.

A Wideband Input Upgrade (order number ATS9462-005) can be purchased for such cases. Bandwidth can be extended to 120 MHz with minimal effect on noise performance.

Note: the wideband input upgrade on the ATS9462 can only be used while in Amplifier Bypass Mode.

Acquisition System

ATS9462 PCI digitizers use a pair of state of the art 180 MS/s, 16-bit ADCs to digitize the input signals. The real-time sampling rate ranges from 180 MS/s down to 1 KS/s. The two channels are guaranteed to be simultaneous, as they share the exact same clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data.

Infinite number of triggers can be captured by ATS9462 while operating in dual-port memory mode.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 32 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

Maximum Sustained Transfer Rate

PCI Express support on different motherboards is not always the same, resulting in significantly different sustained data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

ATS9462 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the bus benchmarking tool provided in AlazarDSO for Windows or AlazarFrontPanel for Linux.

Recommended Motherboards or PCs

Many different types of motherboards and PCs have been benchmarked by AlazarTech. The ones that have produced the best throughput results are listed here: www.alazartech.com/images-media/2246-AlazarTechRecommendedMotherboards.pdf.

On-Board Acquisition Memory

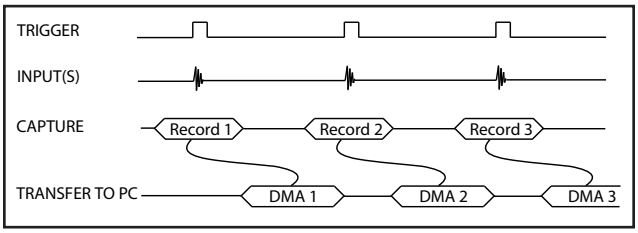
ATS9462 supports on-board memory buffers of 64 Megasamples and 512 Megasamples. There are two distinct advantages of having on-board memory:

First, a snapshot of the ADC data can be stored into this acquisition memory at full acquisition speed without any concern for the bus throughput.

Second, and more importantly, on-board memory can also act as a very deep FIFO between the Analog-to-Digital converters and PCI Express bus, allowing very fast sustained data transfers across the bus, even if the operating system or another motherboard resource temporarily interrupts DMA transfers.

Traditional AutoDMA

In order to acquire both pre-trigger and post-trigger data in a dual-ported memory environment, users can use Traditional AutoDMA.



Data is returned to the user in buffers, where each buffer can contain from 1 to 8191 records (triggers). This number is called RecordsPerBuffer.

As shown in the diagram above, each record is transferred to PC host memory as soon as it is acquired.

Users can also specify that each record should come with its own header that contains a 40-bit trigger timestamp.

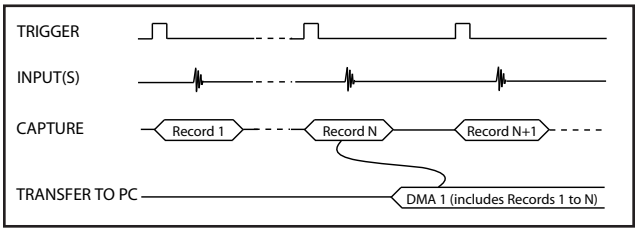
A BUFFER_OVERFLOW flag is asserted if more than 512 buffers have been acquired by the acquisition system, but not transferred to host PC memory by the AutoDMA engine.

While Traditional AutoDMA can acquire data to PC host memory at the maximum sustained transfer rate of the motherboard, a BUFFER_OVERFLOW can occur if more than 512 triggers occur in very rapid succession, even if all the on-board memory has not been used up.

No Pre-Trigger (NPT) AutoDMA

Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.



Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired.

NPT AutoDMA buffers do not include headers. However, users can specify that each record should come with its own footer that contains a 40-bit trigger timestamp. The footer is called NPT Footer.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

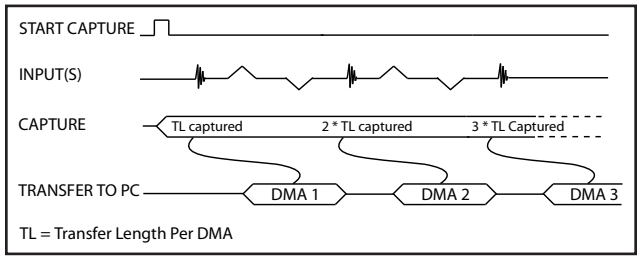
NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCIe bus as soon as the ATS9462 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

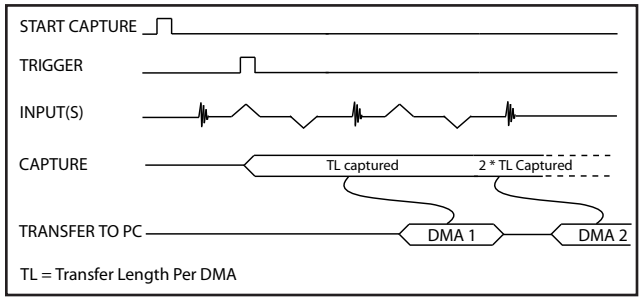
A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

FPGA-Based Input Processing Engine

ATS9462 contains an Altera Stratix II FPGA that manages the datapath, the DDR2 memory interface and PCI Express bus interface.

As part of ongoing product improvement, an Input Processing Engine (IPE) has been introduced in the on-board FPGA, whereby data coming from the on-board A/D converter ICs goes through this IPE before being stored in on-board memory or being DMA'd to host computer memory.

The first part of the IPE consists of an FIR filter that acts as a band-pass filter by default, but can be modified to be low-pass or high-pass filter.

The next part of the IPE applies a windowing function to the acquired data. By default, a Hanning window is used, but user is allowed to download a different function.

Note that the windowing function can only be used for NPT AutoDMA acquisitions with up to 2048-point records.

Software-selectable Bandwidth Limit

A majority of applications for PCI digitizers require oversampling of input signal, i.e. the frequency of the analog signal being digitized is a factor of 5 or 6 lower than the sample rate or even the Nyquist rate.

ATS9462 features a software-controlled bandwidth limit switch, which reduces high-frequency noise and improves signal to noise ratio. This switch is independently selectable for each input channel.

When selected, bandwidth limit switch can reduce the input bandwidth of a particular input to be approximately 20 MHz.

Triggering

The ATS9462 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

While most oscilloscopes offer only one trigger engine, ATS9462 offers two trigger engines (called Engines J and K). This allows the user to combine the two engines using a logical OR, AND or XOR operand.

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

External Trigger Input

ATS9462 external trigger input (TRIG IN) can be set as an analog input with ±5 V or ±1 V full scale input range and 1 MΩ input impedance.

Timebase

Timebase on the ATS9462 can be controlled either by on-board clock sources or by optional External Clock.

On-board clock sources consist of three different oscillators: a 10 MHz TCXO that is multiplied to produce the 180 MHz and 160 MHz sampling rate; a 125 MHz crystal oscillator that provides the 125 MS/s sample rate; and a 100 MHz crystal oscillator that provides 100 MS/s and lower sampling rates.

Sample rates lower than 100 MS/s are achieved by sampling at 100 MS/s and decimating the ADC data stream by an appropriate factor.

Optional External Clock

While the ATS9462 features low-jitter, high-reliability 125 MHz and 100 MHz crystal oscillators and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9462 External Clock option provides an SMA input for an external clock signal.

The input stage of the External Clock circuit is an analog comparator that converts the incoming signal into a PECL clock signal that can be used by the on-board ADCs.

Note that the input impedance for the External Clock input is fixed at 50 Ω. Input coupling for the external clock input is user-programmable between AC and DC coupling.

Fast External Clock

If the user selects Fast External Clock mode, a new sample is taken by the on-board ADCs for each rising (or falling) edge of this External Clock signal.

In order to operate the ADC under optimal conditions, the user must set the appropriate frequency range for the external clock being supplied. The following ranges are supported:

External Clock: 1 MHz < f_{EXT} < 180 MHz

The active edge of the external clock is software-selectable between the rising or falling edge.

Slow External Clock

If the external clock frequency is less than 1 MHz, then users can select Slow External Clock.

Note that Slow External Clock signal must be a 3.3 Volt TTL signal.

In this mode, the on-board ADCs are run at a fixed 125 MS/s sample rate. Each time a rising (or falling) edge is detected on the external clock signal, one sample is stored.

Thus, there can be zero to 8 ns skew between the clock edge and the actual sampling of the signal. This skew can change from sample to sample, so this type of clock should be used only if this jitter is acceptable in your application.

10 MHz Clock Reference

It is possible to generate the sampling clock based on a 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9462 uses an on-board PLL to generate the high-frequency clock. Clock frequencies in the range of 150 MHz to 180 MHz can be generated with a 1 MHz resolution.

AUX Connector - Trigger Output

ATS9462 provides an AUX (Auxiliary) BNC connector that is configured as a Trigger Output connector by default.

When configured as a Trigger Output, AUX BNC connector outputs a 5 Volt TTL signal synchronous to the ATS9462 Trigger signal, allowing users to synchronize their test systems to the ATS9462 Trigger.

When combined with the Trigger Delay feature of the ATS9462, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX Connector - Trigger Enable

Another use of AUX connector is its use as a Trigger Enable Input in imaging applications.

In such applications, users must first configure AUX I/O as a Trigger Enable. A FRAME_START signal should be connected to AUX I/O and LINE_START signal to TRIG IN.

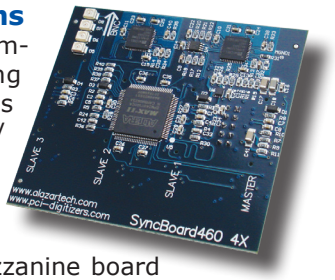
Once armed, ATS9462 will not trigger until a FRAME_START pulse has arrived. It will then accept a certain number of triggers and then wait for the next FRAME_START pulse before accepting any more triggers.

This mechanism guarantees full frame image acquisition.

Calibration

Every ATS9462 digitizer is factory calibrated to NIST- or CNRC-traceable standards. To periodically recalibrate an ATS9462, the digitizer must be shipped back to the factory.

Master/Slave Systems



Up to 8 inputs can be sampled simultaneously using multiple ATS9462 boards configured as a Master/Slave system by using a SyncBoard 9462 of appropriate width.

SyncBoard 9462 is a mezzanine board and plugs into the connector located along the top edge of the ATS9462 boards.

A SyncBoard 9462 uses the clock output from a Master board and delivers copies of that clock to all boards, using equal length traces. Note that no PLL is used for clock buffering, thus ensuring truly simultaneous sampling even if the clock frequency is not constant.

SyncBoard 9462 also allows any of the boards to trigger the entire Master/Slave system.

It should be noted that PCI Express is not a shared bus. As such, the data throughput is not shared between multiple boards in a Master/Slave system

AlazarDSO Software

ATS9462 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

The Stream-To-Memory command in AlazarDSO allows users to stream a large dataset to motherboard memory.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits

AlazarTech provides easy-to-use software development kits for customers who want to integrate the ATS9462 into their own software.

A Windows and Linux compatible software development kit, called ATS-SDK, includes headers, libraries and source code sample programs written in C/C++, C#, Python, MATLAB, and LabVIEW. These programs can fully control the ATS9462 and acquire data in user buffers.

The purchase of an ATS-SDK license includes a subscription that provides the following benefits for a period of 12 months from the date of purchase:

- Download ATS-SDK updates from the AlazarTech website;
- Receive technical support on ATS-SDK.

Customers who want to receive technical support and download new releases beyond this 12 month period should purchase extended support and maintenance (order number ATS-SDK-1YR).

ATS-GPU

ATS-GPU is a software library developed by AlazarTech to allow users to do real-time data transfer from ATS9462 to a GPU card at rates up to 720 MB/s.

Interfacing waveform digitizers to GPUs involves creating a software mechanism to move data from one to the other and back to user buffers. The standard techniques used most often can get the job done, but feature very low data throughput due to software overheads.

AlazarTech designed ATS-GPU to eliminate this software bottleneck so that data can be moved from AlazarTech digitizers to GPUs and from GPUs to user buffers at full PCIe bus speeds. Once the data is available in GPU memory, many types of digital signal processing (DSP) can be done on this data at near-hardware speeds.

ATS-GPU-BASE is supplied with an example user application in source code. The application includes GPU kernels that use ATS-GPU to receive data, do very simple signal processing (data inversion), and copy the processed (inverted) data back to a user buffer. All this is done at the highest possible data transfer rate.

Programmers can replace the data inversion code with application-specific signal processing kernels to develop custom applications.

ATS-GPU-OCT is the optional OCT Signal Processing library for ATS-GPU. It contains floating-point FFT routines that have also been optimized to provide the maximum number of FFTs per second. Kernel code running on the GPU can do zero-padding, apply a windowing function, do a floating-point FFT, calculate the amplitude and convert the result to a log scale. It is also possible to output phase information.

FFTs can be done on triggered data or on continuous gapless stream of data. It is also possible to do spectral averaging. Our benchmarks showed that it was possible to do 175,000 FFTs per second when capturing data in dual-channel mode and using a NVIDIA® Quadro® P5000 GPU.

ATS-GPU-NUFFT is an extension of ATS-GPU-OCT that allows non-uniform FFTs to be performed on data acquired uniformly in time domain using a fixed sampling rate. For SS-OCTs where the wave-length does not vary linearly in time, a fixed sampling rate results in data that is non-uniformly dis-tributed in frequency domain. ATS-GPU-NUFFT allows linearized FFTs to be performed on such data.

ATS-GPU supports 64-bit Windows and 64-bit Linux for CUDA®-based development.

Support for Windows

Windows support for ATS9462 includes Windows 10, Windows 8.x, Windows 7 SP1 with security update KB3033929 (SHA-2 Code Signing Support), Windows Server 2012, Windows Server 2010, and Windows Server 2008 R2.

Microsoft support for Windows 7 and Windows Server 2008 R2 ended on January 14, 2020. As such, AlazarTech ceased development on Windows 7 and Windows Server 2008 R2 as of this date. We will continue to support customers using Windows 7 and Windows Server 2008 R2 until December 31, 2020. After this date, no support will be provided.

Due due to lack of demand and due to the fact that Microsoft no longer supports these operating systems, AlazarTech no longer supports Windows XP, Windows Vista, and Windows Server 2008.

Linux Support

AlazarTech offers Dynamic Kernel Module Support (DKMS) drivers for the following Linux distributions: Ubuntu, Debian, and RHEL®.

AlazarTech DKMS drivers may work for other Linux distributions but they have not been tested and technical support may be limited.

Users can download the DKMS driver for their specific distribution by choosing from the available drivers here:

ftp://release@ftp.alazartech.com/outgoing/linux

A GUI application called AlazarFrontPanel that allows simple data acquisition and display is also provided.

ATS-SDK includes source code example programs for Linux, which demonstrate how to acquire data programmatically using a C compiler.

Based on a minimum annual business commitment, the Linux driver source code license (order number ATS9462-LINUX) may be granted to qualified OEM customers for a fee. For release of driver source code, a Non-Disclosure Agreement must be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

Extended Warranty

The purchase of an ATS9462 includes a standard one (1) year parts and labor warranty. Customers may extend their warranty by ordering the appropriate Extended Warranty:

ATS9462-061 for ATS9462-64M

ATS9462-062 for ATS9462-512M

This must be purchased before expiration of the standard warranty (or before expiration of an Extended Warranty). Extended Warranties can only be purchased while there is a valid warranty in place.

AlazarTech reserves the right to limit the number of warranty extensions for any product.

Get your warranty end date by registering your product at: www.alazartech.com/en/my-account/my-products/.

Export Control Classification

According to the Export Controls Division of Government of Canada, ATS9462 is currently not controlled for export from Canada. Its export control classification is N8, which is equivalent to ECCN EAR99. ATS9462 can be shipped freely outside of Canada, with the exception of countries listed on the Area Control List and *Sanctions List*. Furthermore, if the end-use of ATS9462, in part or in its entirety, is related to the development or deployment of weapons of mass destruction, AlazarTech is obliged to apply for an export permit.

RoHS Compliance

ATS9462 is fully RoHS compliant, as defined by Directive 2015/863/EU (RoHS 3) of the European Parliament and of the Council of 31 March 2015 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

All manufacturing is done using RoHS-compliant components and lead-free soldering.

EC Conformity

ATS9462 conforms to the following standards:

Electromagnetic Emissions:
CISPR 32:2015/AMD1:2019 /
EN 55032:2015/A11:2020 (Class A):
Information Technology Equipment (ITE). Radio disturbance characteristics. Limits and method of measurement: EN 61000-3-2:2014, EN 61000-3-3:2013.

Electromagnetic Immunity:
CISPR 24:2010 / EN55024:2010:
Information Technology Equipment Immunity characteristics — Limits and methods of measurement.

Safety:
IEC 62368-1:2014 / EN 62368-1:2014+A11:2017:
Audio/video, information and communication technology equipment - Part 1: Safety requirements.

ATS9462 also follows the provisions of the following directives: 2014/35/EU (Low Voltage Equipment); 2014/30/EU (Electromagnetic Compatibility).

FCC & ICES-003 Compliance

ATS9462 has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15, subpart B of the FCC Rules, and the Canadian Interference-Causing Equipment Standard ICES-003 issue 7 October 2020.

Processing Using Multiple CPU Cores

Programmers can take advantage of multiple cores available in modern CPUs to speed up signal processing.

Benchmarks have shown that a quad-core CPU can perform real-time averaging at a rate of 1.0 GB/s and only use up 20% of CPU cycles. Increasing the number of cores or decreasing the sample rate reduces CPU usage even further.

One of the main applications of using multiple cores to do signal processing is Quantum Computing and Spectroscopy applications, where each record contains partial information about the signal of interest and a large number of records must be accumulated to gather a representative dataset.

System Requirements

Personal computer with at least one free x4, x8 or x16 PCI Express (v1.0a or v1.1 or v2.0) slot, 512 MB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12 V	1.2 A, typical
+3.3 V	1.1 A, typical

Physical

Size	Single slot, half length PCI Express card (4.4 inches x 7.8 inches excluding the connectors protruding from the front panel)
Weight	250 g

I/O Connectors

CH A, CH B, TRIG IN, AUX I/O	BNC female connectors
ECLK	SMA female connector

Environmental

Operating temperature	0 to 55 degrees Celsius
Storage temperature	-20 to 70 degrees Celsius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	16 bits
Bandwidth (-3 dB)	
DC-coupled:	DC - 65 MHz for all ranges, except ±4 V ±4 V: DC - 50 MHz
AC-coupled lower cut-off frequency:	
1 MΩ:	10 Hz
50 Ω:	100 kHz
Number of channels	2, simultaneously sampled
Maximum sample rate	180 MS/s single shot
Minimum sample rate	1 KS/s single shot for internal clocking
Full scale input ranges	
1 MΩ input impedance:	±200 mV, ±400 mV, ±800 mV, ±2 V, ±4 V, ±8 V, and ±16 V, software-selectable
50 Ω input impedance:	±200 mV, ±400 mV, ±800 mV, ±2 V, and ±4 V, software-selectable
DC accuracy	±2% of full scale in all ranges
Input coupling	AC or DC, software-selectable
Input impedance	50 Ω or 1 MΩ ±1% in parallel with 50 pF ±10 pF, software-selectable
Input protection	
1 MΩ	±28 V (DC + peak AC for CH A, CH B and EXT only without external attenuation)
50 Ω	±4 V (DC + peak AC for CH A, CH B and EXT only without external attenuation)

Acquisition Memory System

Memory size	64 MB or 512 MB
Record length	Software-selectable with 32-point resolution. Record length must be a minimum of 256 points and maximum of the on-board memory size for single-port memory operation. There is no upper limit on the maximum record length in data streaming mode.
Number of records	Software-selectable from a minimum of 1 to a maximum of infinite number of records
Pre-trigger depth	Up to 2048 points in NPT mode (with firmware version 23 and higher)
Post-trigger depth	Record Length – Pre-Trigger Depth

Amplifier Bypass Mode

Standard feature	Yes
DIP switch selectable	Yes, independently for each channel
Input range	Approx. 550 mV rms
Input coupling	DC, irrespective of the input coupling setting for the channel
Input impedance	50 Ω, irrespective of the input impedance setting for the channel
Input bandwidth (-3 dB)	85 MHz

Optional Wideband Input

Analog bandwidth using Amplifier Bypass Mode	120 MHz (-3 dB)

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal sample rates	180 MS/s, 160 MS/s, 125 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100 KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal clock accuracy	±2 ppm for 180 MS/s & 160 MS/s ±25 ppm for 125 MS/s and lower

Dynamic Parameters

Typical values measured using a randomly selected ATS9462 with Amplifier Bypass Mode. Input was provided by an HP8656A signal generator, followed by a 9-pole, 1 MHz band-pass filter (TTE Q36T-1M-100K-50-720B). Input frequency was set at 1 MHz and output amplitude was 520 mV rms, which was approximately 95% of the full scale input.

SNR	72.9 dB
SINAD	72.3 dB
THD	-83 dB
SFDR	-82 dB

Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.

Optional ECLK (External Clock) Input

Input impedance	50 Ω
Input coupling	AC or DC, software-selectable
Fast External Clock	
Signal level	500 mV_{P-P} to 2 V_{P-P}
Maximum frequency	180 MHz
Minimum frequency	1 MHz
Sampling edge	Rising or falling, software-selectable
Decimation factor	Software-selectable from 1 to 100,000
Slow External Clock	
Signal Level	3.3 V LVTTL
Maximum frequency	10 MHz
Minimum frequency	DC

Optional 10 MHz Reference PLL Input

Signal Level	500 mV_{P-P} to 2 V_{P-P} or 3.3 V LVTTL
Input impedance	50 Ω
Input coupling	AC coupled
Input frequency	10 MHz ± 0.1 MHz
Maximum frequency	10.1 MHz
Minimum frequency	9.9 MHz
Sampling clock freq.	150 MHz to 180 MHz with 1 MHz resolution

Triggering System

Mode	Edge triggering with hysteresis
Comparator type	Digital comparators for internal (CH A, CH B) triggering and analog comparators for TRIG IN (External) triggering
Number of trigger engines	2
Trigger engine combination	Engine J, engine K, J OR K, software-selectable
Trigger engine source	CH A, CH B, EXT, Software or None, independently software-selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	65 MHz
Trigger delay	Software-selectable from 0 to 9,999,999 sampling clock cycles
Trigger timeout	Software-selectable with a 10 µs resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input impedance	1.01 MΩ ±10% in parallel with 50 pF ±10 pF
Bandwidth (-3 dB)	
DC-coupled	DC - 25 MHz
AC-coupled	10 Hz - 25 MHz
Input range	±5 V or ±1 V, software-selectable
DC accuracy	±10% of full scale input
Input protection	±28 V (DC + peak AC without external attenuation)
Coupling	AC or DC, software-selectable

Auxiliary I/O (AUX I/O)

Signal direction	Input or Output, software-selectable. Trigger Output by default
Output types:	Trigger Output, Pacer (programmable clock) Output, Software-controlled Digital Output
Input types:	Trigger Enable Software readable Digital Input
Output	
Amplitude:	5 Volt TTL
Synchronization:	Synchronized to rising edge of sampling clock
Input	
Amplitude:	3.3 Volt TTL (5 Volt compliant)
Input coupling:	DC

Materials Supplied

ATS9462 PCI Express Card

ATS9462 Install Disk on USB flash drive

Certification and Compliances

RoHS 3 (Directive 2015/863/EU) Compliance

CE Marking — EC Conformity

FCC Part 15 Class A / ICES-003 Class A Compliance

All specifications are subject to change without notice

ORDERING INFORMATION

ATS9462-64M	ATS9462-002
ATS9462-512M	ATS9462-003
ATS9462: External Clock Upgrade	ATS9462-004
ATS9462: Wideband Input Upgrade	ATS9462-005
ATS9462: SyncBoard 2x	ATS9462-006
ATS9462: SyncBoard 4x	ATS9462-007
ATS9462: FIFO-only to 64M Upgrade	ATS9462-010
ATS9462: FIFO-only to 512M Upgrade	ATS9462-011
ATS9462: 64M to 512M Upgrade	ATS9462-012
ATS9462-64M: One Year Extended Warranty	ATS9462-061
ATS9462-512M: One Year Extended Warranty	ATS9462-062
Software Development Kit License + 1 Year Subscription (Supports C/C++, Python, MATLAB, and LabVIEW)	ATS-SDK
ATS-GPU-BASE: GPU Streaming Library License + 1 Year Subscription	ATSGPU-001
ATS-GPU-OCT: Signal Processing Library License + 1 Year Subscription (requires ATSGPU-001)	ATSGPU-101
ATS-GPU-NUFFT: ATS-GPU-OCT Extension for fixed-frequency sampled data License + 1 Year Subscription (requires ATSGPU-001 & ATSGPU-101)	ATSGPU-201

Manufactured By:

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DATASHEET REVISION HISTORY

Changes from version 1.5H (Jan 2020) to version 1.5I	Section, Page
Updated section *ATS-GPU* and added paragraph on ATS-GPU-NUFFT	ATS-GPU, pg. 6
Updated Linux Support (RHEL) and added new DKMS drivers	Linux Support, pg. 6
Updated product registration URL	Extended Warranty, pg. 7
Updated standards and directives	EC Conformity, pg. 7
Updated year of FCC and ICES-003 standards	FCC & ICES-003 Compliance, pg. 7
Added Auxiliary I/O input coupling (DC)	Auxiliary I/O (AUX I/O), pg. 9
Updated software descriptions and added order number for ATS-GPU-NUFFT	Ordering Information, pg. 10

Changes from version 1.5G (May 2019) to version 1.5H	Section, Page
Changed *Sampling Rate* column to *Max. Sample Rate*	Feature Table, pg. 1
Added AlazarFrontPanel (for Linux) as benchmarking tool	Maximum Sustained Transfer Rate, pg. 2
Removed qualified metrology lab as option for recalibrating ATS9462	Calibration, pg. 5
Specified Windows 7 version support, re-ordered list of operating systems, and added end-of-support notice for Windows 7 and Windows Server 2008 R2	Support for Windows, pg. 6
Specified Linux distributions: CentOS, Debian, and Ubuntu	Linux Support, pg. 6
Clarified specifications by separating Fast and Slow External Clock Changed fast ext. clock signal from "±200 mV to ±1 V" to "500 mV_{P-P} to 2 V_{P-P}" Removed sine wave requirement	Optional ECLK (External Clock) Input, pg. 9
Changed signal level from "±200 mV sine wave or 3.3 V LVTTL" to "500 mV_{P-P} to 2 V_{P-P} or 3.3 V LVTTL"	Optional 10 MHz Reference PLL Input, pg. 9
Corrected Output types (removed Busy Output and added Pacer Output)	Auxiliary I/O (AUX I/O), pg. 9

Changes from version 1.5F (Jan 2019) to version 1.5G	Section, Page
Updated ATS-GPU data transfer rate and benchmarks (FFTs per second and GPU)	ATS-GPU, pg. 6
Removed *ATS-GMA* section as this product is being discontinued	ATS-GMA, pg. 6
Added section *Extended Warranty*	Extended Warranty, pg. 6
Specified that listed Pre-trigger depth applies to NPT mode	Acquisition Memory System, pg. 8
Added External Clock input coupling	Optional ECLK (External Clock) Input, pg. 9
Updated Trademark information	pg. 9
Removed ATS-GMA order numbers (ATSGMA-001, ATSGMA-101)	Ordering Information, pg. 10

Changes from version 1.5E (Sept 2018) to version 1.5F	Section, Page
Updated *Sanctions List* URL	Export Control Classification, pg. 7
Updated Trademark information	pg. 9

Changes from version 1.5D (Jan 2018) to version 1.5E	Section, Page
Updated RoHS Compliance to RoHS 3	Global change
Updated product image	pg. 1
Clarified Operating System Support	Feature Table, pg. 1
Added note: Wideband Input Upgrade can only be used while in Amplifier Bypass Mode	Wideband Input Upgrade, pg. 2
Correction of trigger engines: changed to J and K (instead of X and Y)	Triggering, pg. 4
Added *External Trigger Input* section	External Trigger Input, pg. 4
Added information on ATS-SDK license	Software Development Kits, pg. 5
Specified 64-bit version for Windows and Linux support	ATS-GPU, pg. 6
Added *ATS-GMA* section	ATS-GMA, pg. 6
Added list of supported Microsoft Windows versions	Support for Windows, pg. 6
Added *Acquisition Memory System* section	Acquisition Memory System, pg. 8
Added Maximum Amplitude: 2 V_{P-P}	Optional ECLK (External Clock) Input, pg. 9
Added "PLL" to section name for clarity, corrected Input Frequency tolerance, and added Max. and Min. Frequencies	Optional 10 MHz Reference PLL Input, pg. 9

DATASHEET REVISION HISTORY

Changes from version 1.5D (Jan 2018) to version 1.5E (continued)	Section, Page
Corrected Trigger Engine Combination	Triggering System, pg. 9
Replaced *TRIG OUT Output* section with *Auxiliary I/O (AUX I/O)*	Auxiliary I/O (AUX I/O), pg. 9
Added Trademark information	pg. 9
Added subscription length for ATS-SDK, ATSGPU-001, ATSGPU-101 Added products ATSGMA-001, ATSGMA-101	Ordering Information, pg. 10

Changes from version 1.5C (Oct 2017) to version 1.5D	Section, Page
Added note about NPT Footers	No Pre-Trigger (NPT) AutoDMA, pg. 3
Added CNRC as calibration standard	Calibration, pg. 5
Added -BASE and -OCT to ATS-GPU description for clarity	ATS-GPU, pg. 5
Corrected size of card	Physical, pg. 7
Updated email address	Manufactured By, pg. 8

Changes from version 1.5B (Oct 2017) to version 1.5C	Section, Page
Updated description for product ATSGPU-001 & ATSGPU-101	Ordering Information System, pg. 8

Changes from version 1.5A (Oct 2017) to version 1.5B	Section, Page
Added DC-coupled bandwidth for ±4 V range (DC - 50 MHz)	Acquisition System, pg. 7
Changed the way AC-coupled bandwidth is specified. Now showing AC-coupled lower cut-off frequency	Acquisition System, pg. 7
Removed Bandwidth flatness specification	Acquisition System, pg. 7

Changes from version 1.5 (Sept 2017) to version 1.5A	Section, Page
Corrected full scale input range for Amplifier Bypass Mode to ±800 mV	Amplifier Bypass Mode, pg. 2

Changes from version 1.4 (Nov 2013) to version 1.5	Section, Page
Added Python to list of SDK supported languages, and Support for Windows & Linux	Features, pg. 1
Removed deprecated basic model (FIFO-only) with no on-board memory	Overview, pg. 1
Added Python & LabVIEW to list of supported languages for ATS-SDK, removed ATS-VI	Overview, pg. 1
Specified that Attenuating probes are not included	Analog Input, pg. 2
Removed section *FIFO-Only Model*; product deprecated	FIFO-Only Model, pg. 2
Removed section on deprecated AlazarDSO plug-in: *Calibration Software*	Calibration Software, pg. 5
Modified AlazarDSO description	AlazarDSO Software, pg. 5
Removed deprecated items: *Optional Stream-To-Disk Software*; *Optional Acquire At Time Plug-In*	AlazarDSO Software, pg. 5
New section *Software Development Kits* to replace sections: *ATS-SDK Software Development Kit* and *ATS-VI Software Development Kit*	Software Development Kits, pg. 5
Replaced *GPU Based Signal Processing* section with new *ATS-GPU* section	ATS-GPU, pg. 5
Replaced section *ATS9462-Linux Software Development Kit* with new *Linux Support* section	Linux Support, pg. 6
Added Export Control Classification information	Export Control Classification, pg. 6
Added section on RoHS compliance	RoHS Compliance, pg. 6
Added section on EC Conformity	EC Conformity, pg. 6
Added section on FCC & ICES-003 Compliance	FCC & ICES-003 Compliance, pg. 6
Updated External Trigger Input Impedance to 1.01 MΩ ±10%	TRIG IN (External Trigger) Input, pg. 8
Updated list of Certification and Compliances	Certification and Compliances, pg. 8
Corrected product name for ATS-SDK	Ordering Information, pg. 8
Removed ATS-VI (ATS-SDK now supports LabVIEW)	Ordering Information, pg. 8
Removed products ATS9462-001, ATS9462-009, ATS9462-Linux, ATSGPU-WIN ATS-DSO-STR, ATS-DSO-AAT, ATS-DSO-CAL, ATS-DSO-PDK	Ordering Information, pg. 8
Added products ATS9462-061, ATS9462-062, ATSGPU-001, ATSGPU-101	Ordering Information, pg. 8